F I G. 1

AC DRIVING TYPE PLASMA DISPLAY APPARATUS
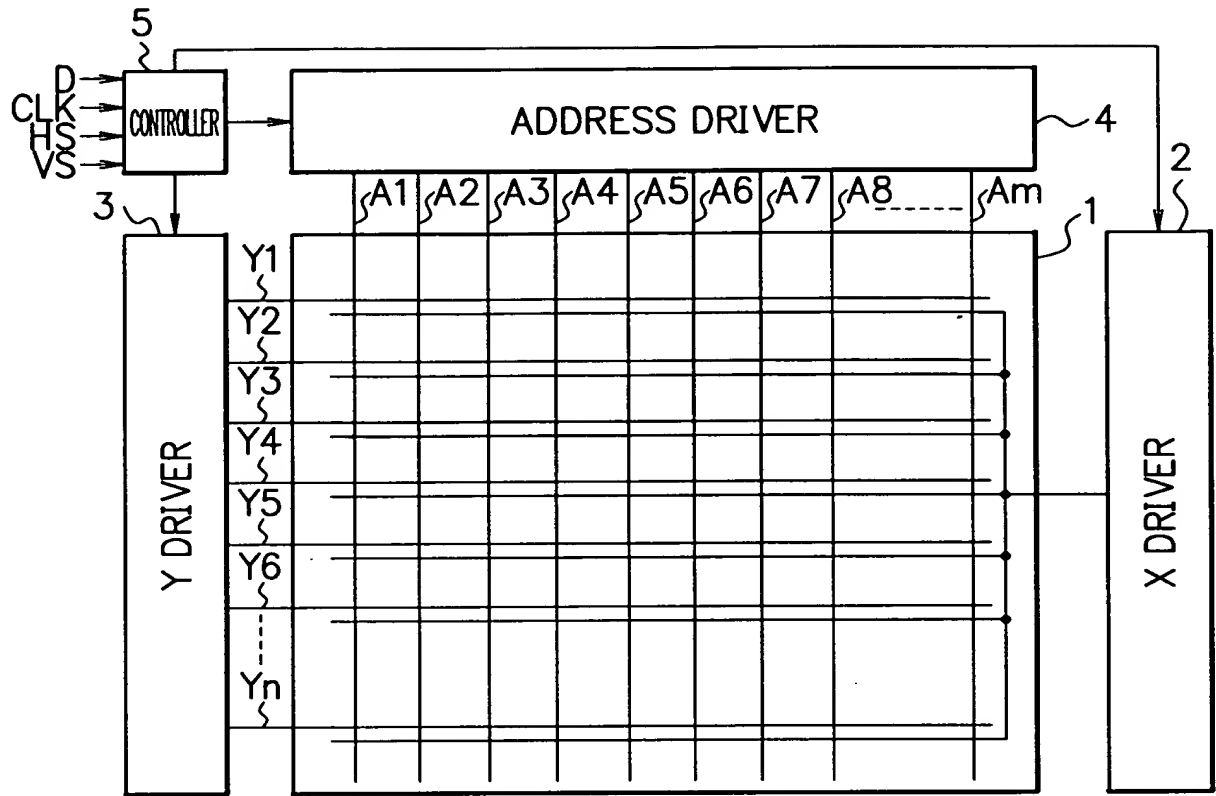
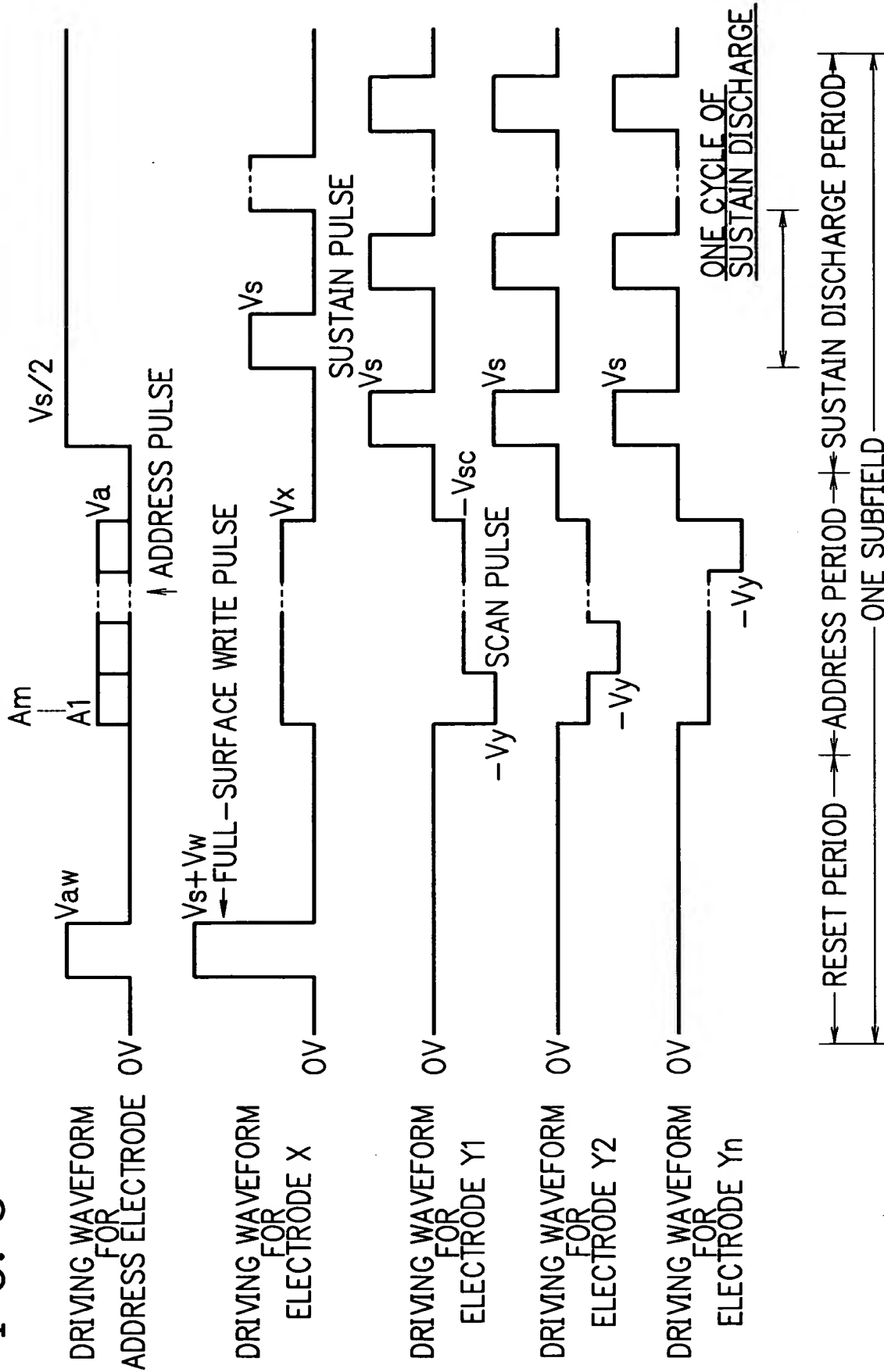# F I G. 2

SECTIONAL STRUCTURE OF CELL
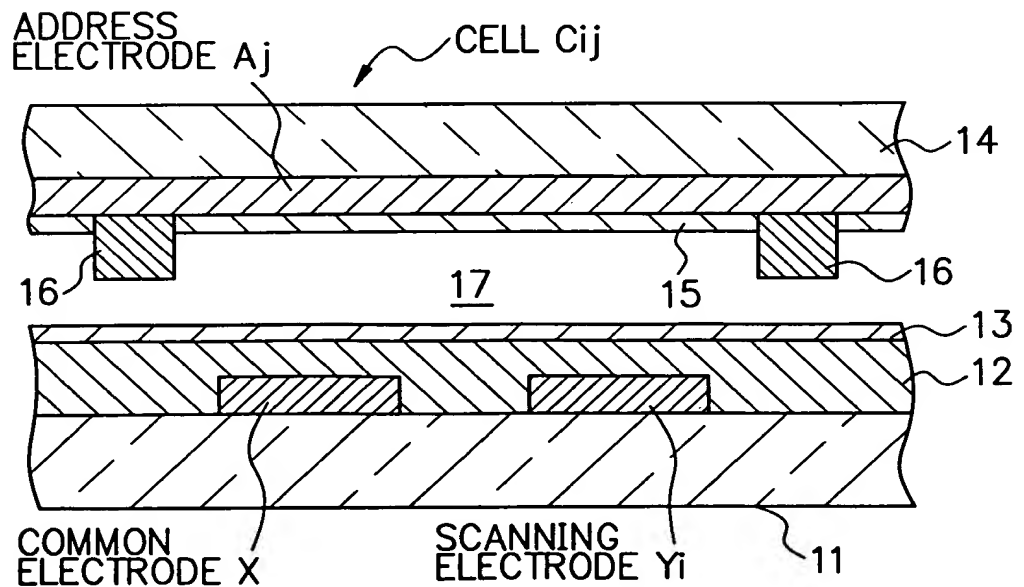
FIG. 3

WAVEFORM CHART SHOWING CONVENTIONAL DRIVING METHOD

DRIVING WAVEFORM FOR ADDRESS ELECTRODE

V_{aw}

$V_s/2$

Am

A1

V_a

ADDRESS PULSE

0V

DRIVING WAVEFORM FOR ELECTRODE X

$V_s + V_w$

FULL-SURFACE WRITE PULSE

V_x

V_s

V_s

SUSTAIN PULSE

0V

DRIVING WAVEFORM FOR ELECTRODE Y1

V_s

$-V_{sc}$

SCAN PULSE

$-V_y$

0V

DRIVING WAVEFORM FOR ELECTRODE Y2

V_s

$-V_y$

0V

DRIVING WAVEFORM FOR ELECTRODE Yn

V_s

$-V_y$

0V

ONE CYCLE OF SUSTAIN DISCHARGE

RESET PERIOD — ADDRESS PERIOD — SUSTAIN DISCHARGE PERIOD

ONE SUBFIELD

FIG. 4

CONVENTIONAL SUBFIELD STRUCTURE

ADDRESS PERIOD | SUSTAIN DISCHARGE PERIOD | RESET PERIOD
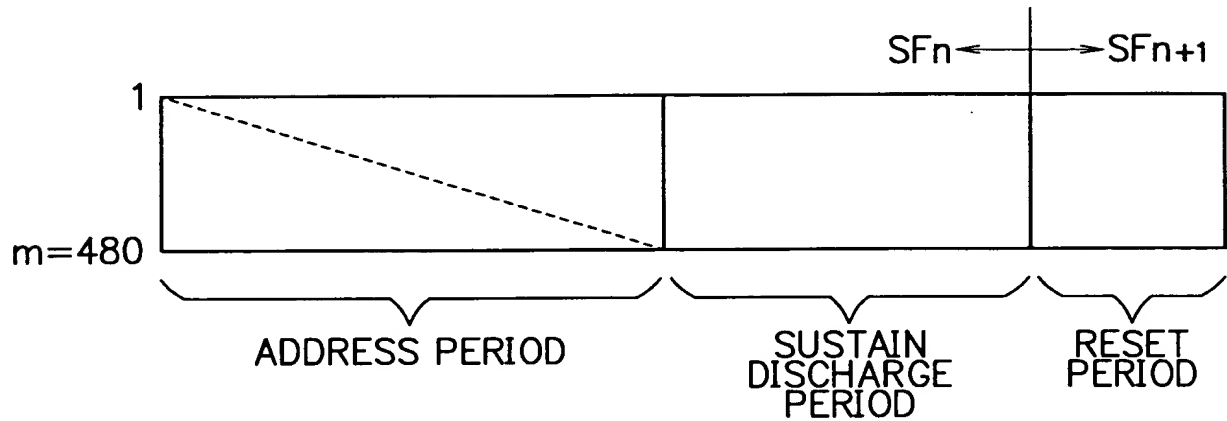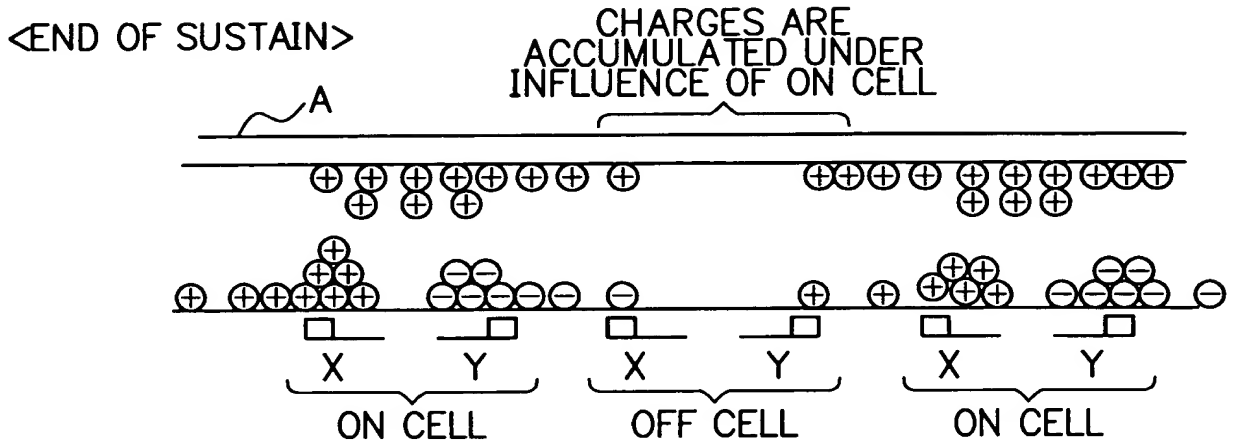
FIG. 5

WAVEFORM CHART SHOWING EXAMPLE OF PDP DRIVING METHOD

CHARGE ACCUMULATION STATE

F I G. 6A

<END OF SUSTAIN>

CHARGES ARE
ACCUMULATED UNDER
INFLUENCE OF ON CELL

A

| X | Y | X | Y | X | Y |

ON CELL   OFF CELL   ON CELL

F I G. 6B

<ERASE>

A

| X | Y | X | Y | X | Y |

ON CELL
IN SUSTAIN
C1

OFF CELL
IN SUSTAIN
C2
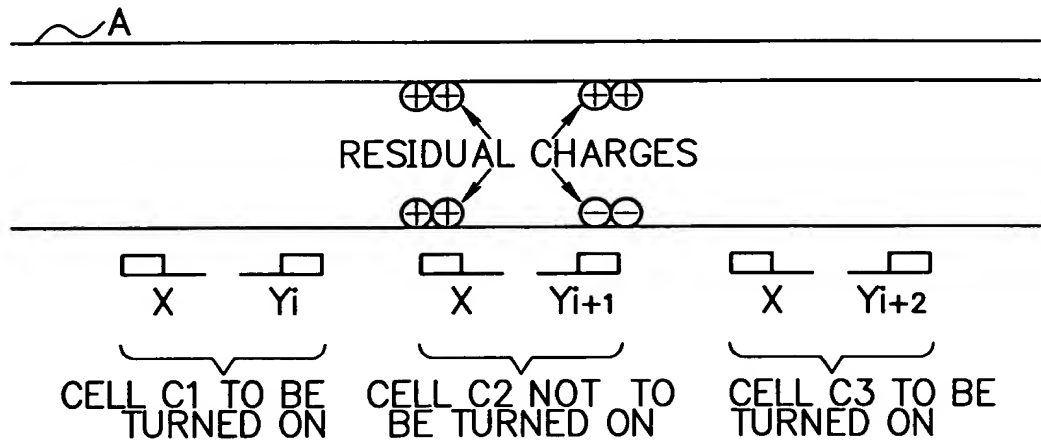
ON CELL
IN SUSTAIN
C3

F I G. 6C

A

ERASE   ERASE

| X | Y | X | Y | X | Y |
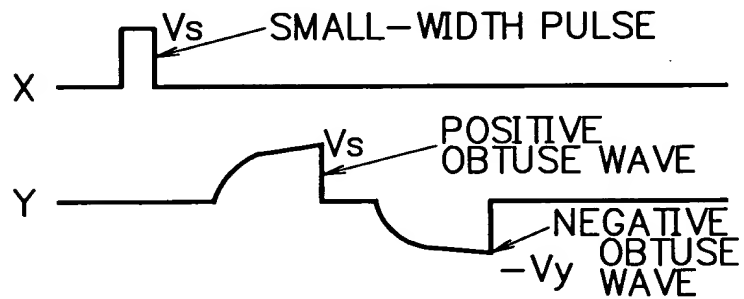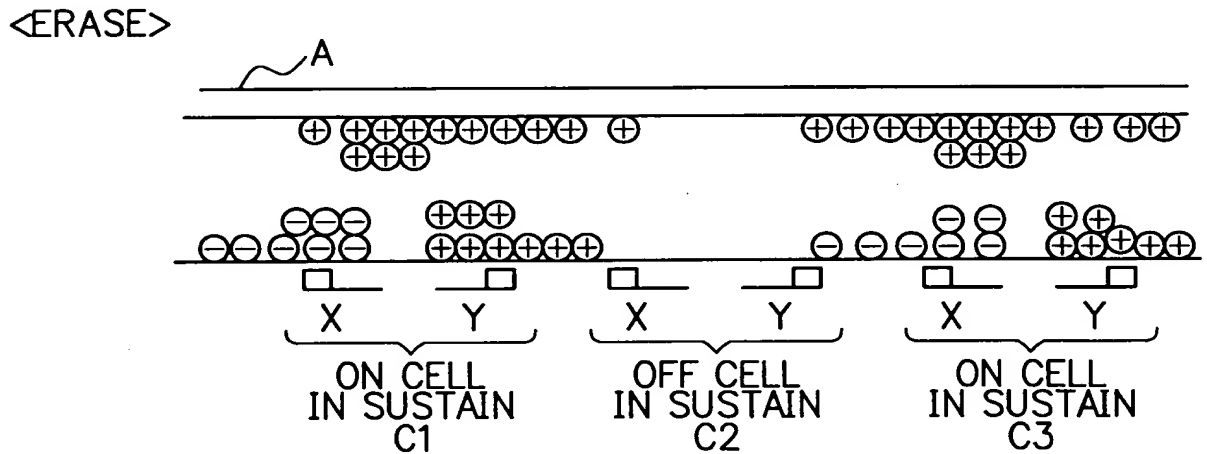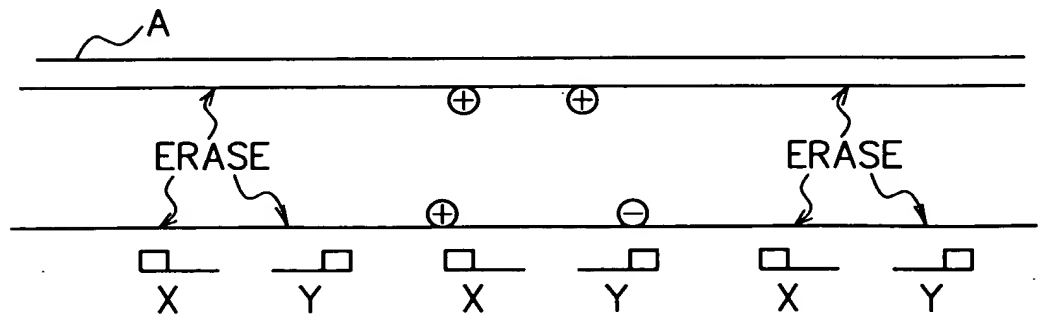
F I G. 7

CHARGE ACCUMULATION STATE IN ADDRESS PERIOD

<ADDRESS PERIOD>

RESIDUAL CHARGES

X   Yi   X   Yi+1   X   Yi+2

CELL C1 TO BE TURNED ON   CELL C2 NOT TO BE TURNED ON   CELL C3 TO BE TURNED ON

ADDRESS   Va

X   Vx

DISCHARGE   MISS DISCHARGE   DISCHARGE

Yi   −Vy

Yi+1   −Vy

Yi+2   −Vy
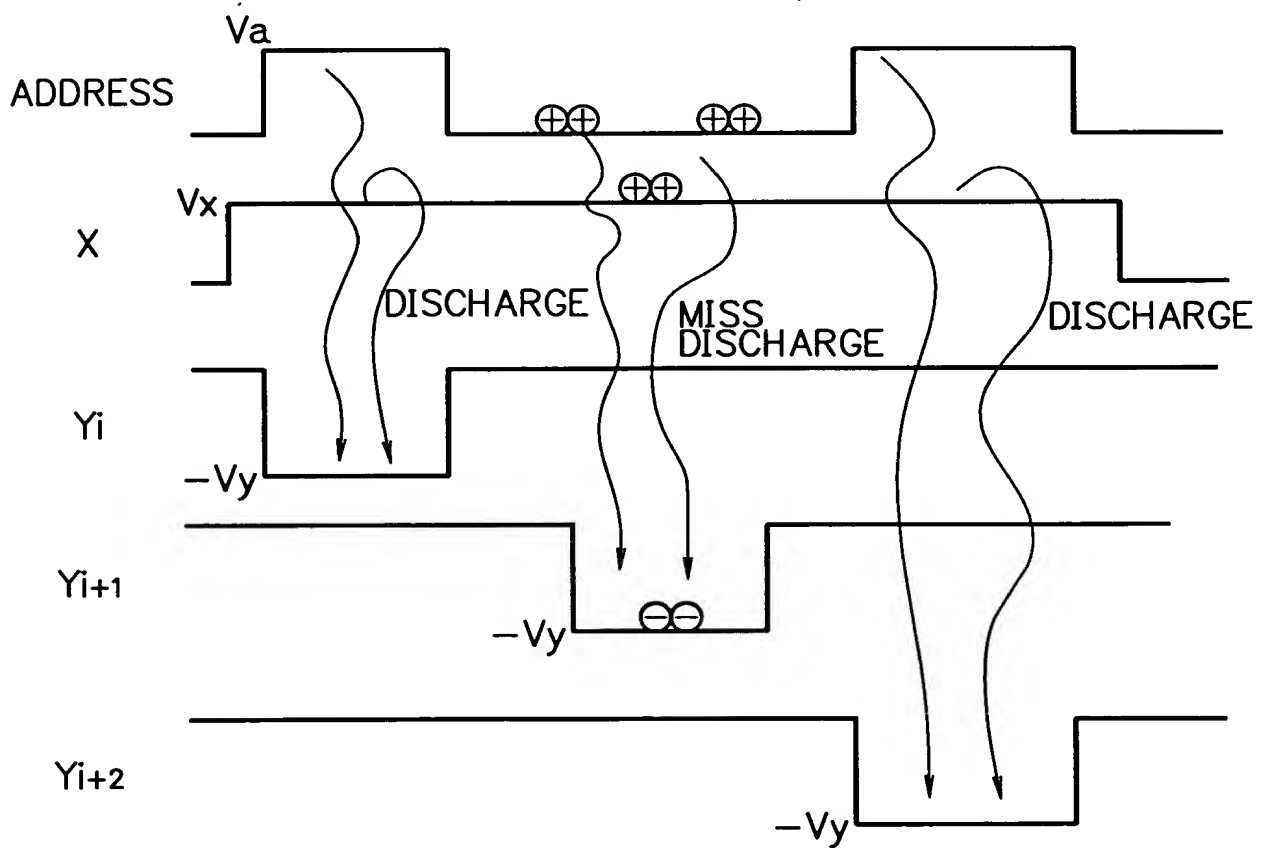
FIG. 8

SUBFIELD STRUCTURE IN EMBODIMENT

SFn ← | → SFn+1

1

m=480

ADDRESS PERIOD

SUSTAIN PERIOD

ERASE 1 ERASE 2

RESET PERIOD

F I G. 9

PDP DRIVING WAVEFORM IN EMBODIMENT

DRIVING WAVEFORM
FOR ADDRESS ELECTRODE

DRIVING WAVEFORM
FOR ELECTRODE X

DRIVING WAVEFORM
FOR ELECTRODE Y

ADDRESS PULSE

SUSTAIN PULSE

SCAN PULSE

ONE CYCLE OF
SUSTAIN DISCHARGE

FIRST ERASE   SECOND ERASE
DISCHARGE   DISCHARGE
PERIOD   PERIOD

RESET PERIOD

ADDRESS PERIOD   SUSTAIN DISCHARGE PERIOD

ONE SUBFIELD
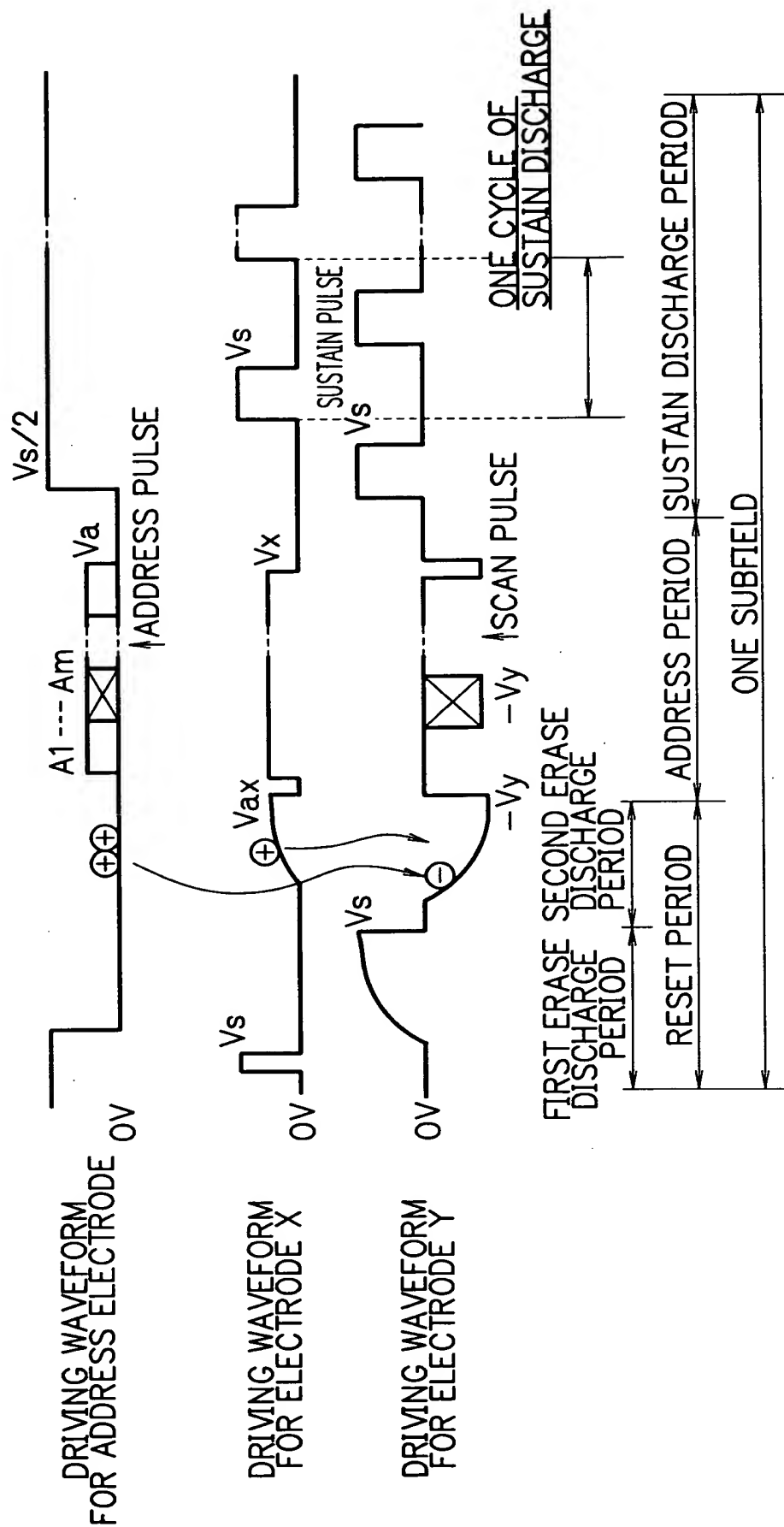
ILLUSTRATION FOR VARIABLE Vax

F I G. 10A

VARIABLE Vx

Vax

ELECTRODE X   0V

ELECTRODE Y   0V

$-Vy$

F I G. 10B

Vx

VARIABLE Vax

ELECTRODE X   0V

ELECTRODE Y   0V

$-Vy$
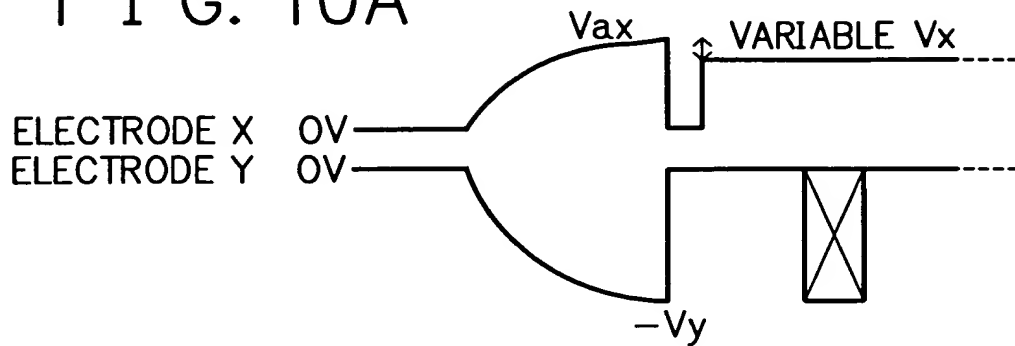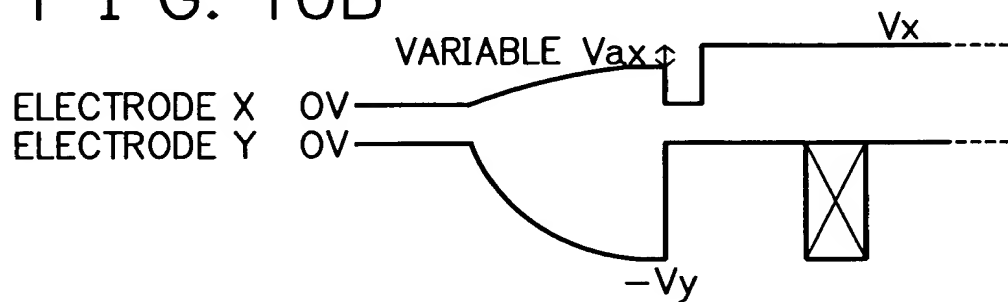
F I G. 11

HARDWARE ARRANGEMENT FOR VARIABLE Vax

21

22

1

23

Ry

24

Y

X

Rx

$-Vy$

Va
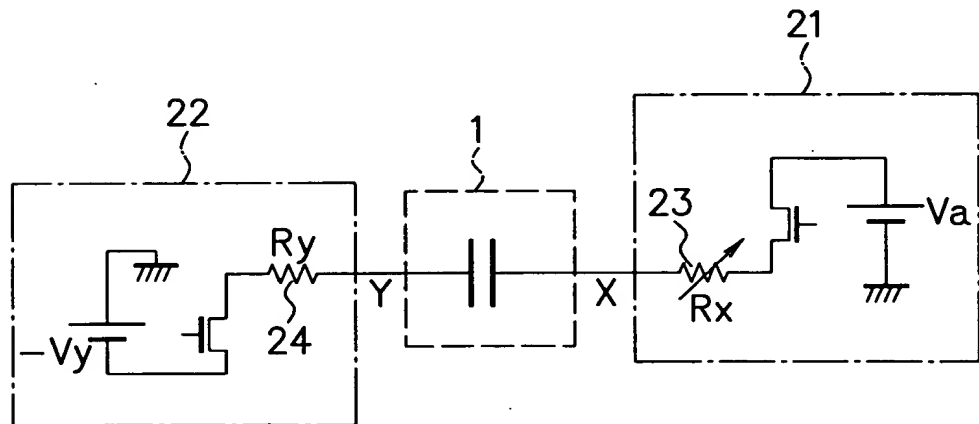
CHARGE ACCUMULATION STATE IN EMBODIMENT

F I G. 12A
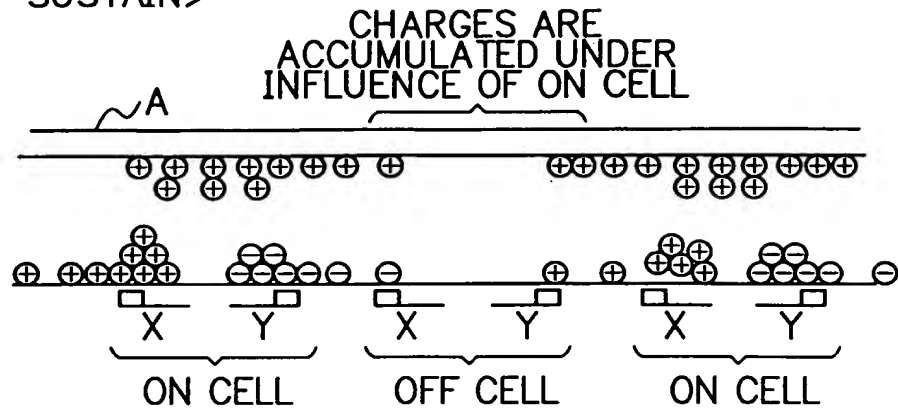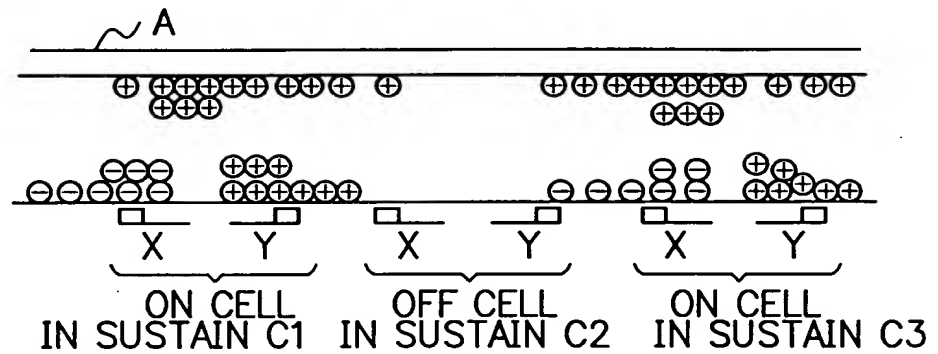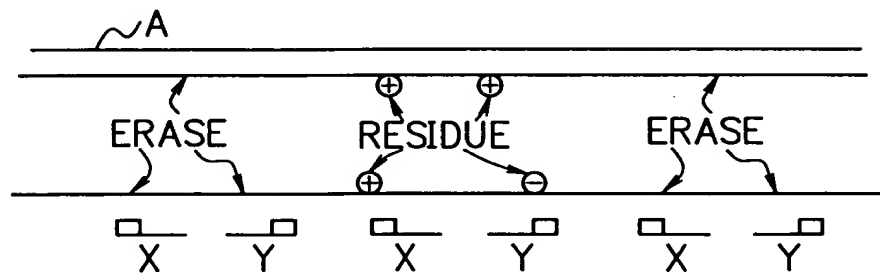
<END OF SUSTAIN>

CHARGES ARE
ACCUMULATED UNDER
INFLUENCE OF ON CELL

~A

X   Y   X   Y   X   Y

ON CELL   OFF CELL   ON CELL

F I G. 12B

<ERASE>

~A

X   Y   X   Y   X   Y

ON CELL   OFF CELL   ON CELL
IN SUSTAIN C1   IN SUSTAIN C2   IN SUSTAIN C3

F I G. 12C

~A

ERASE   RESIDUE   ERASE

X   Y   X   Y   X   Y

F I G. 12D

~A

RESIDUAL CHARGES ARE REMOVED

X   Yi   X   Yi+1   X   Yi+2

CELL C1 TO   CELL C2 NOT TO   CELL C3 TO
BE TURNED ON   BE TURNED ON   BE TURNED ON
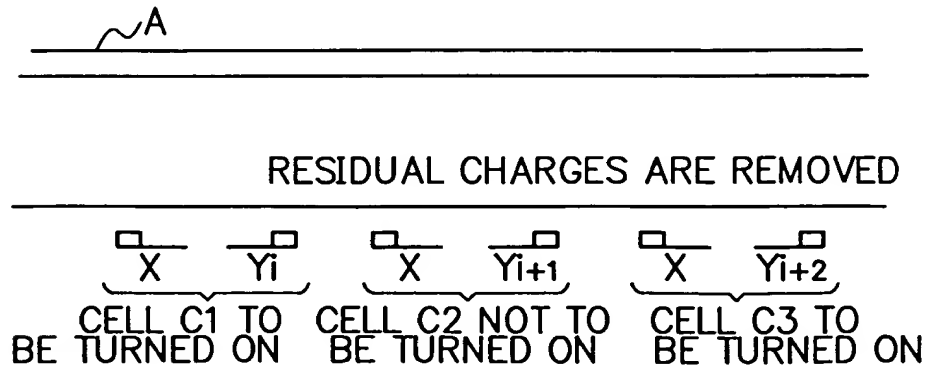
F I G. 13

ANOTHER EXAMPLE OF PDP DRIVING WAVEFORM

DRIVING WAVEFOEM
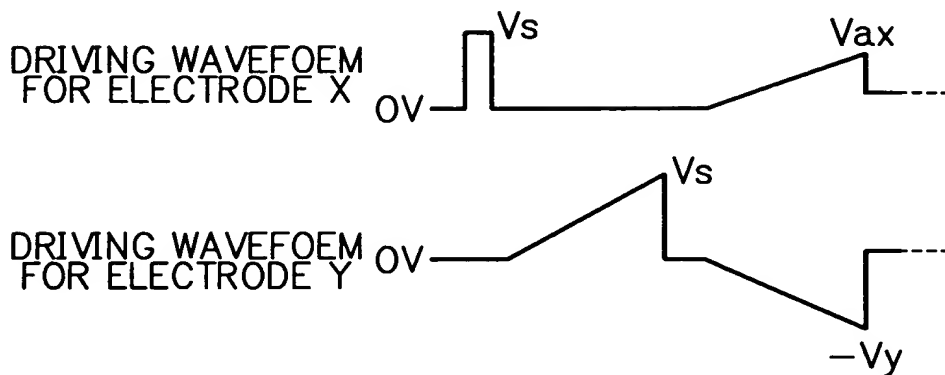FOR ELECTRODE X

DRIVING WAVEFOEM
FOR ELECTRODE Y

F I G. 14

ANOTHER EXAMPLE OF RISE TIMING OF
SECOND POSITIVE OBTUSE WAVE

DRIVING WAVEFOEM
FOR ELECTRODE X

DRIVING WAVEFOEM
FOR ELECTRODE Y